In the Claims:

1. (Currently Amended) In a process of fabricating a narrow channel width PMOSFET device, the improvement of affecting reduction of negative bias temperature instability by use of F_2 side wall implantation, comprising:

a) forming a shallow trench isolation (STI) region in a substrate having a pad oxide and a nitride layer on its surface;

~~b) forming a gate on a gate oxide in said substrate;~~

~~e~~b) forming a liner layer in said shallow trench isolation region and subjecting said liner layer to oxidation to form a STI liner oxidation layer;

~~d~~c) implanting F_2 into ~~side walls~~ upper top corners of said STI liner oxidation layer at a large tilted angle in sufficient amounts to affect reduction of negative bias temperature instability and enhance gate oxidation at the STI corner after a high density plasma fill of said STI F_2 implanted liner oxidation layer; and

~~e~~d) filling the STI ~~F2~~ F_2 implanted structure from step ~~d~~c) with a high density plasma (HDP) fill to affect reduction of negative bias temperature instability and enhance gate oxidation at the STI corner.

2. (Original) The process of claim 1 wherein said substrate is Si.

3. (Original) The process of claim 2 wherein said liner oxidation layer is SiO_2.

4. (Original) The process of claim 2 wherein said liner oxidation layer is SiON.

5. (Original) The process of claim 3 wherein said large tilted angle is from about 10 to about 30 degrees with reference to the Y axis.

6. (Original) The process of claim 4 wherein said large tilted angle is from about 10 to about 30 degrees with reference to the Y axis.

7. (Currently Amended) The process of claim ~~of~~ 5 wherein said sufficient amount of F_2 is a dose of from about 5×10^{12} to about $1x10^{14}cm^2$.

8. (Original) The process of claim 6 wherein said sufficient amount of F_2 is a dose of from about 5×10^{12} to about $1x10^{14}cm^2$.

9. (Original) The process of claim 7 wherein said high density plasma (HDP) fill is a HDP oxide fill.

10. (Original) The process of claim 8 wherein said high density plasma (HDP) fill is a HDP oxide fill.

11. (New) A method of forming a semiconductor structure, the method comprising:

providing a semiconductor substrate;

forming a trench within the semiconductor substrate, the trench including upper top corners, ~~side walls~~;

after forming the trench, implanting fluorine into the upper top corners, ~~side walls~~ of the trench, the implanting being performed at a large tilted angle; and

after implanting fluorine, filling the trench with an insulating material.

12. (New) The method of claim 11 and further comprising lining the trench side walls with an oxide layer prior to implanting fluorine.

13. (New) The method of claim 11 wherein providing a semiconductor substrate comprises providing a semiconductor substrate having a pad oxide formed over a portion thereof and a nitride layer formed over the pad oxide.

14. (New) The method of claim 11 wherein implanting fluorine comprises implanting fluorine in sufficient amounts to affect reduction of negative bias temperature stability and enhance gate oxidation at the STI corner.

15. (New) The method of claim 11 wherein filling the trench comprises performing a high density plasma oxide deposition.

16. (New) The method of claim 11 wherein the large tilted angle is from about 10 to about 30 degrees with reference to the Y axis.

17. (New) The method of claim 11 and further comprising forming a P-channel transistor in a region of the substrate adjacent the filled trench.

18. (New) The method of claim 11 wherein implanting fluorine comprises implanting F_2 at a dose of from about $5x10^{12}$ to about $1x10^{14}cm^2$.